REMARKS

Claims 43 and 70 are amended, claims 1-42 are canceled, and no claims are added; as a result, claims 43-88 are now pending in this application.

Applicant cancels method claims 1-42 without prejudice or disclaimer. Applicant intends to file a divisional application directed to these claims.

Election/Restriction

Applicant respectfully requests consideration of claims 70-88. For example, claim 70 recites, in part, an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal; and an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal. This is essentially the same subject matter as claim 43. Accordingly, if claim 43 is found allowable, then claim 70 is also allowable. Claim 71 should also be considered. Claim 71 includes, in part, the similar subject matter as found in claim 43. If claim 43 is found allowable, then claims 71-74 are also allowable. Applicant submits that consideration of claims 70-88 would not place additional burdens on the examiner. Reconsideration of the assertion of constructive election is requested.

§103 Rejection of the Claims

Claims 43-54 were rejected under 35 USC § 103(a) as being unpatentable over Butler et al. (U.S. Patent No. 5,392,241) in view of Uruma et al. (U.S. Patent No. 5,313,431). Applicant respectfully traverses.

Claim 43 recites, in part, "an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal." Applicant can not find this feature in Butler or Uruma. Reconsideration is requested.

The Office Action cites col. 7, lines 12-15 of Butler as teaching the immediately-above feature of claim 43. Col. 7, lines 12-15 of Butler recites "Sense amplifier timing chain 80 also receives input from an address decode circuit 82, which itself is controlled by row/column

addresses received from controller 74." This portion of Butler clearly lacks any specific reference to a sense amplifier signal as recited in claim 43.

Claim 43 further recites, in part, "an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal." Applicant can not find this feature in Butler or Uruma. Reconsideration is requested.

The Office Action cites col. 7, lines 15-24 of Butler as teaching the immediately-above feature of claim 43. Col. 7, lines 15-24 of Butler recites

> Timing chain 80 outputs SETBL and SETBLN signals, along with their compliments, to primary and secondary set devices of memory array 76. One of ordinary skill in the art can readily implement a timing chain to provide these signals, which are depicted and described herein. Also output from address decoder 82 are word line address signal "WL" and write switching signal "Y". An I/O interface 84 receives/-transmits data between memory circuit 72 and controller 74, and is coupled to memory array 76.

This portion of Butler clearly lacks any specific reference to a timing circuit that includes an output connected to an address decoder. Moreover, this portion of Butler clearly lacks any specific reference to the timing circuit activating the address decoder based on the at least one input signal as recited in claim 43.

The Office Action states that although not expressly stated as such, the sense amp timing chain 80, upon receiving an input, causes activation of the address decoder. Applicant respectfully traverses this assertion. First, the timing chain 80 receives input from the address decoder. The address decoder 82 must be active to send a signal to the timing chain 80. Applicant can not find any disclosure in Butler that states any activation dependence of the address decoder 82 on the timing chain 80. Second, applicant submits that Butler teaches away from the present invention as recited in claim 43. Specifically, Butler states that the sense amplifier timing chain 80 receives input from the address decode circuit 82. Applicant does not see how the timing amplifier chain 80 can activate the address decoder if the address decoder provides the input to the timing amplifier chain 80.

As applicant can not find a timing circuit in Butler that includes an input adapted to receive a sense amplifier signal or an output connected to the address decoder as recited in claim 43, applicant submits that claims 43-45 and 47-48 are allowable.

Applicant requests clarification of the present rejection as the Office Action simultaneously indicates that claim 46 is rejected as obvious and is allowable.

Applicant requests clarification of the present obviousness rejection, which is a combination of Butler and Uruma. The Office Action at pages 3 and 4 discusses Butler as teaching elements of claims 43-54. There is no discussion of Uruma or how one of skill in the art would be motivated to combine Butler with Uruma to reject claims 43-53. Clarification is required for appeal.

Claim 49 is believed to be allowable for substantially similar reasons as stated above with regard to claim 43. Moreover, claim 49 is similar to claim 46, which was indicated as allowable. Reconsideration of claim 49 and its dependent claims 50-54 is requested.

The Examiner appears to reject claims 43-53 based only on Butler. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found Butler. Since all the elements of the claim are not found in the reference, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of official notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

The Office Action took official notice of the "limitations" of claims 44-45, 47-48, and 50-53. Applicant respectfully traverses this official notice and requests the Examiner to provide a reference that describes such an element. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Claim 54 was rejected under 35 USC § 103(a) as being unpatentable over Butler et al. in view of Uruma et al. Applicant traverses for at least the reasons stated above with regard to claim 49.

Allowable Subject Matter

Claim 46 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 46 is so rewritten. Allowance of claim 46 is requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at 612-349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

RAMANDEEP S. SAWHNEY

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
612-349-9587

Date 5 May '03

By _____
Timothy B Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 5th day of May 2003

Tina Kohart
Name

Signature